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TITLE : HV430FHB-F90

Preliminary Product Specification

Rev.P0

HeFei BOE Display Technology Co., Ltd

REVISION HISTORY

(√) Preliminary specification

( ) Final specification

Revision No.	Page	Description of changes	Date	Prepared
P0	-	Initial Release	2019.05.30	Wang Kai

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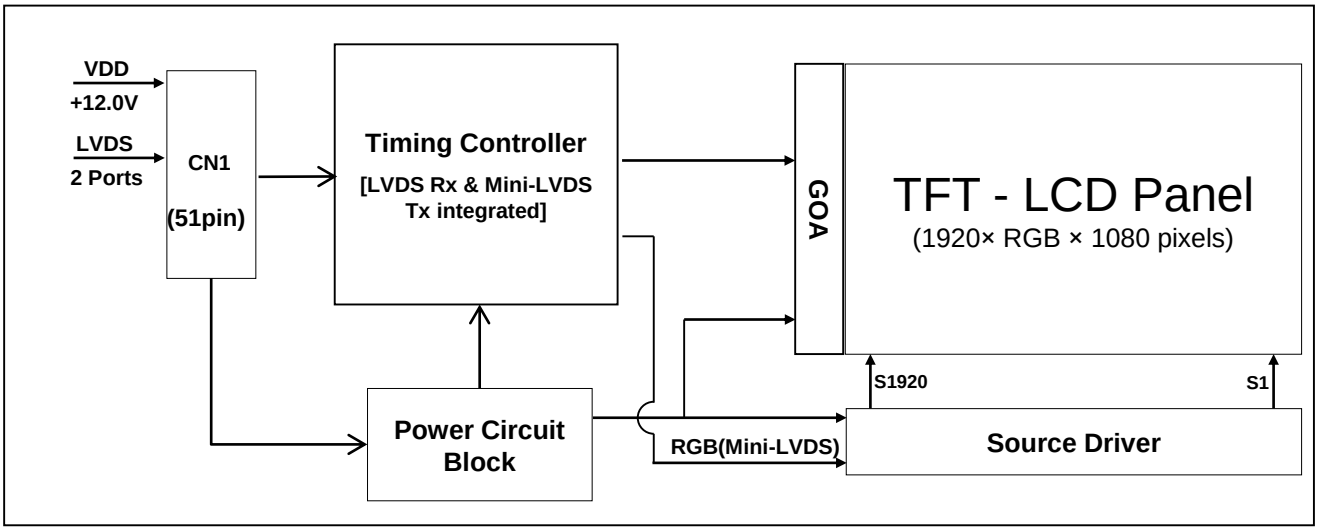
1.0 GENERAL DESCRIPTION

1.1 Introduction

HV430FHB-F90 is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This open cell has a 42.5 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel is adapted for a low reflection and higher color type.



1.2 Features

- mini-LVDS interface with 2port 3pair
- High-speed response
- Low color shift image quality
- 8-bit Source Driver IC
- High luminance and contrast ratio, low reflection and wide viewing angle
- ADS technology is applied for high display quality
- RoHS compliant

1.0 GENERAL DESCRIPTION

1.3 Application

- Home Alone Multimedia TFT-LCD TV
- Display Terminals for Control System
- Ultra High Definition TV(UHD TV)
- AV application Products

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Active area	940.896(H) × 529.254(V)	mm	
Number of pixels	1920(H) ×1080(V)	pixels	
Pixel pitch	163.35(H) ×490.05(V)	um	
Pixel arrangement	Pixels RGB Vertical stripe		
Display colors	1.07G (8bits+FRC)	colors	
Display mode	Transmission mode, Normally Black		
Open Cell Transmittance	6.30 (Typ.)	%	At center point with BOE BLU
Weight	1510 (Typ.)	gram	
Power Consumption	TBD	Watt	
Surface Treatment	Haze 1%, 3H, Anti-glare treatment (Front Polarizer) Clear(Bottom Polarizer)		

2.0 ABSOLUTE MAXIMUM RATINGS

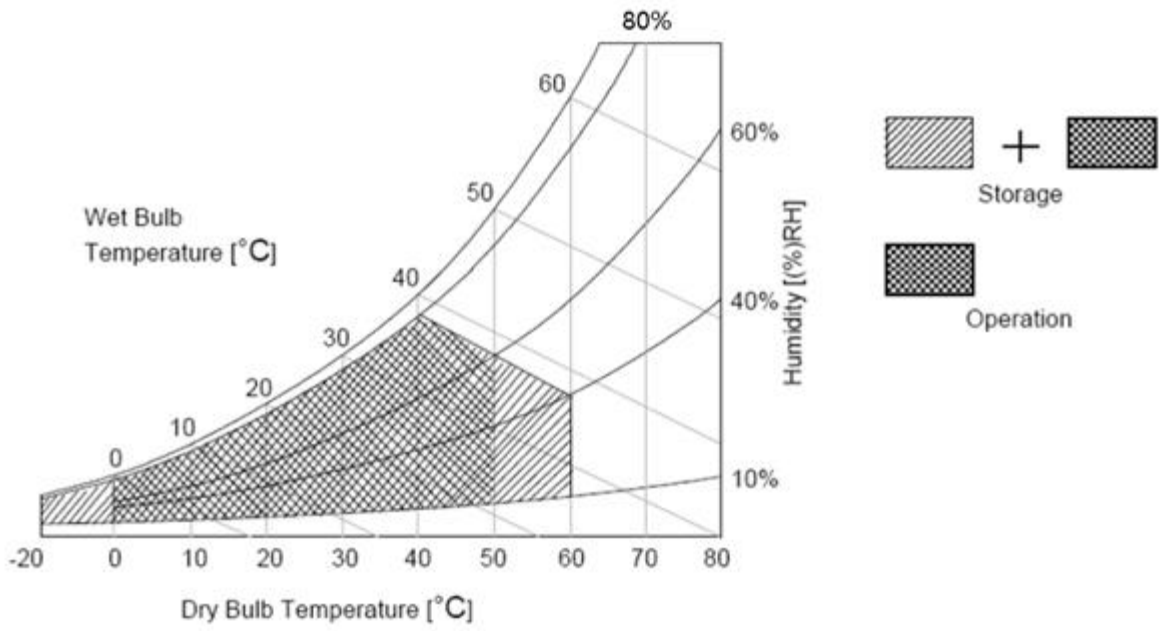
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Absolute Maximum Ratings >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	VSS-0.3	13.2	V	Ta = 25 ℃
Operating Temperature	T_{OP}	0	+50	℃	Note 1
Storage Temperature	T_{SUR}	-20	+60	℃	
	T_{ST}	-20	+60	℃	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Note 2 : Wet bulb temperature should be 39 ℃ max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

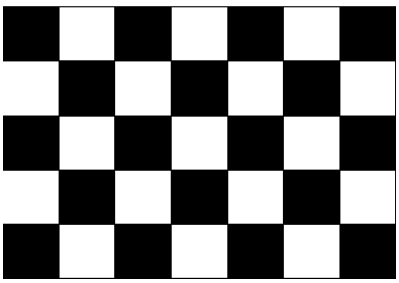
< Table 3. Open Cell Electrical Specifications >

[Ta =25±2 ℃]

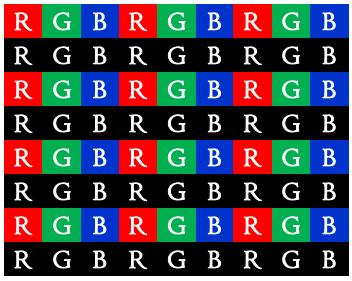
Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	13.2	Vdc	
Power Supply Ripple Voltage		VRP	-	-	600	mV	
Power Supply Current		IDD	-	TBD	TBD	A	Note 1
Power Consumption		PDD		TBD	TBD	Watt	
Rush current		IRUSH	-	-	TBD	A	Note 2
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	+100	-	+300	mV	
	Differential Input Low Threshold Voltage	VLVTL	-300	-	-100	mV	
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
CMOS Interface	Input High Threshold Voltage	VIH	2.31	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.99	V	

Note 1 : The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=12.0V.

a) Typ: Mosaic 7X5(L0/L255)



b) Max : Horizontal 1 Line (L0/L255)



c) Flicker Test Pattern



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min).

3.0 ELECTRICAL SPECIFICATIONS

3.2 IC Characteristics

< Table 4. TCON Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
TCON Surface Temperature	T_{TS}	-	-	TBD	℃	Note

Note 1 : Any point on the TCON surface must be less than TBD under any conditions.

Note 2 : This test condition is based on BOE module.

< Table 5. Driver Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
Driver Surface Temperature	T_{DS}	-	-	125	℃	Note

Note 3 : Any point on the driver surface must be less than 125 ℃ under any conditions.

Note 4: This test condition is based on BOE module.

< Table 6. PMIC Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
PMIC Surface Temperature	T_{PS}	-	-	100	℃	Note

Note 5 : Any point on the PMIC surface must be less than 100 ℃ under any conditions.

Note 6: This test condition is based on BOE module.

3.0 ELECTRICAL SPECIFICATIONS

3.3 VCOM tuning SOP

Slave Address byte

0	1	0	0	0	0	A0	R/W

MSB LSB

A0	Read	Write
Low	01000001b (41h)	01000000b (40h)

Write Multiple Bytes To DR (DAC Register):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 40h. (The iML8973 address 0100000b and R/W bit = Low)
iML8973 will acknowledge a bit for this byte.

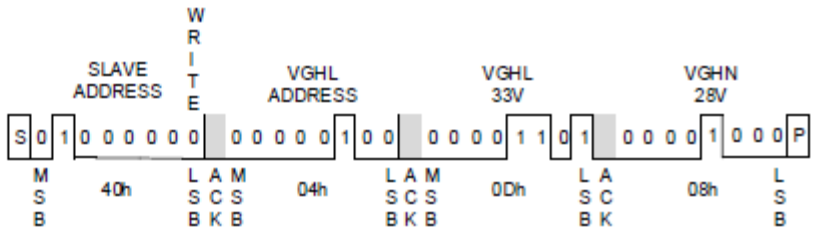
Step 3: Send DR address (ex.04h, address of VGHL Set)
iML8973 will acknowledge a bit for this byte.

Step 4: Send the data to be written to the DR (ex.0Dh, V_{GHL}=33V) iML8973 will acknowledge a bit for this byte.

Step 5: Master continues sending the other bytes to be written to the DRs. iML8973 will acknowledge a bit for each byte and DR address will automatically increase.

Step 6: Master sends Stop Condition.

Example: Writing 0Dh(33V), 08h (28V) to the DR address 04h and 05h.



S: Start Condition, P: Stop Condition, X: Don't Care.

: Master to Slave, :Slave to Master

VCOM Register Address byte

Address	Bit	Name	Symbol								
25h	[7:0]	02h	VCOM	-	-	-	-	-	-	VC[9]	VC[8]
26h	[7:0]	00h		VC[7]	VC[6]	VC[5]	VC[4]	VC[3]	VC[2]	VC[1]	VC[0]

3.3 VCOM tuning SOP

Read Multiple Data From DAC Register (DR):

Step 1: Master sends Start Condition.

Step 2: Master sends the value 40h. (The iML8973 address 0100000b and R/W bit = Low)
iML8973 will acknowledge a bit for this byte.

Step 3: Send Control Register (CR) address (FFh)
iML8973 will acknowledge a bit for this byte.

Step 4: Send the instruction 00XXXXX0b (X: Don't care, ex. 00h) to specify that the data is read from the DR. iML8973 will acknowledge a bit for this byte.

Step 5: Master sends Stop Condition.

Step 6: Master sends Start Condition.

Step 7: Master sends the value 40h. (The iML8973 address 0100000b and R/W bit = Low)
iML8973 will acknowledge a bit for this byte.

Step 8: Send specified DR address to be read (ex.04h, address of VGHL) iML8973 will acknowledge a bit for this byte.

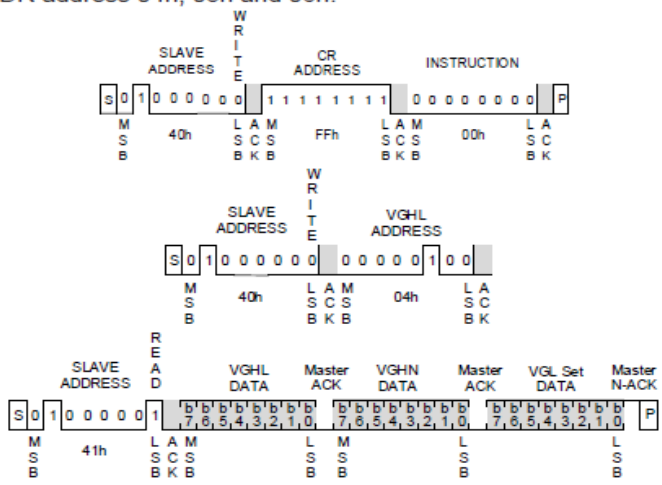
Step 9: Master sends Start Condition (Repeated Start Condition, instead of Stop Condition)

Step 10: Master sends the value 41h. (The iML8973 address 0100000b and R/W bit = High)
iML8973 will acknowledge a bit for this byte.

Step 11: Master continues read the data from DR and acknowledges a bit for each byte. But, master not-acknowledges after received the last reading data. The DR address will automatically increase.

Step 12: Master sends Stop Condition.

Example: Reading data from DR address 04h, 05h and 06h.



S: Start Condition, P: Stop Condition, X: Don't Care.

□: Master to Slave, ▯:Slave to Master

4.0 INTERFACE CONNECTION

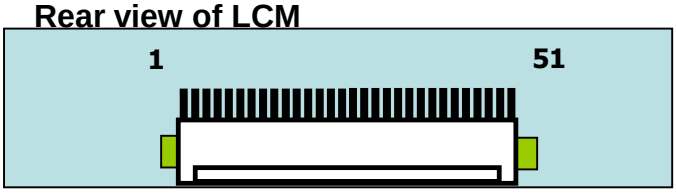
4.1 LVDS CN (51Pin) Connector :.

< Table 7. Open Cell Input Connector Pin Configuration >

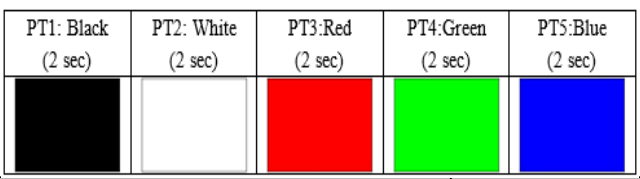
Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No Connection	27	NC	No Connection
2	SDA	SDA	28	LV0NR	LVDS Receiver Signal(-)
3	SCL	SCL	29	LV0PR	LVDS Receiver Signal(+)
4	NC	No Connection	30	LV1NR	LVDS Receiver Signal(-)
5	NC	No Connection	31	LV1PR	LVDS Receiver Signal(+)
6	NC	No Connection	32	LV2NR	LVDS Receiver Signal(-)
7	SELLVDS	High: JEIDA Low or Open: VESA	33	LV2PR	LVDS Receiver Signal(+)
8	NC	No Connection	34	GND	Ground
9	NC	No Connection	35	LVCKNR	LVDS Receiver Clock Signal(-)
10	NC	No Connection	36	LVCKPR	LVDS Receiver Clock Signal(+)
11	GND	Ground	37	GND	Ground
12	LV0NL	LVDS Receiver Signal(-)	38	LV3NR	LVDS Receiver Signal(-)
13	LV0PL	LVDS Receiver Signal(+)	39	LV3PR	LVDS Receiver Signal(+)
14	LV1NL	LVDS Receiver Signal(-)	40	NC	No Connection
15	LV1PL	LVDS Receiver Signal(+)	41	NC	No Connection
16	LV2NL	LVDS Receiver Signal(-)	42	NC	No Connection
17	LV2PL	LVDS Receiver Signal(+)	43	NC	No Connection
18	GND	Ground	44	GND	Ground
19	LVCKNL	LVDS Receiver Clock Signal(-)	45	GND	Ground
20	LVCKPL	LVDS Receiver Clock Signal(+)	46	GND	Ground
21	GND	Ground	47	NC	No Connection
22	LV3NL	LVDS Receiver Signal(-)	48	VDD	Power Supply +12.0V
23	LV3PL	LVDS Receiver Signal(+)	49	VDD	Power Supply +12.0V
24	NC	No Connection	50	VDD	Power Supply +12.0V
25	NC	No Connection	51	VDD	Power Supply +12.0V
26	NC	No Connection			

Note : NC(Not Connected) : These pins are only used for BOE internal operations.

Rear view of LCM



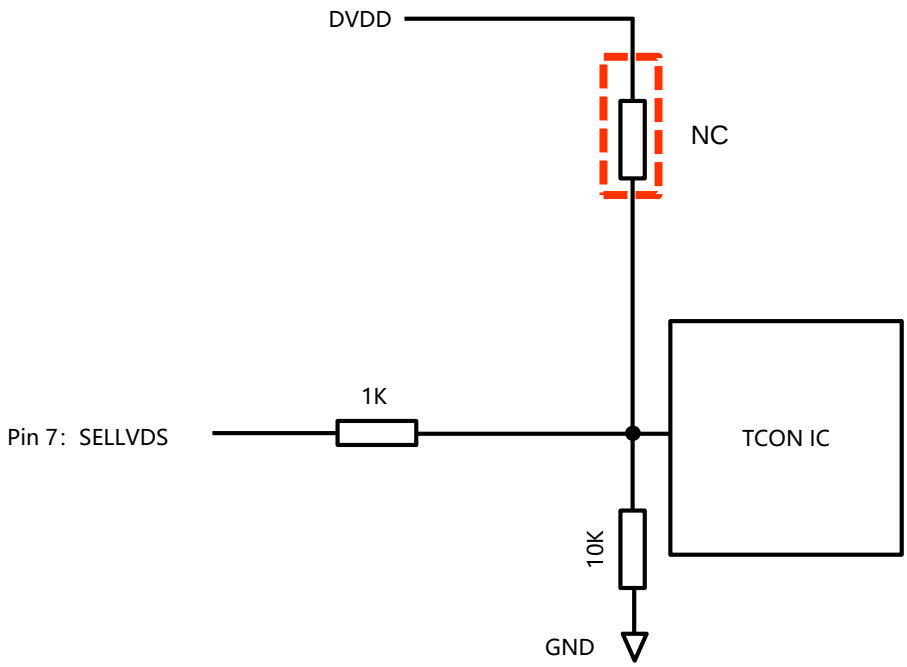
BIST Pattern



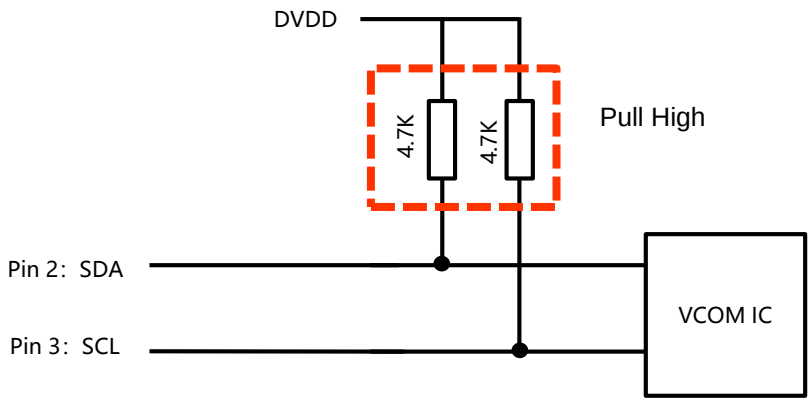
Notes : 1. NC (Not Connected) : This pins are only used for BOE internal operations.

2.BIST : This pin is used for selecting display pattern mode when input DE or input CLOCK quits toggling.

3. Circuit Block Diagram of SELLVDS.



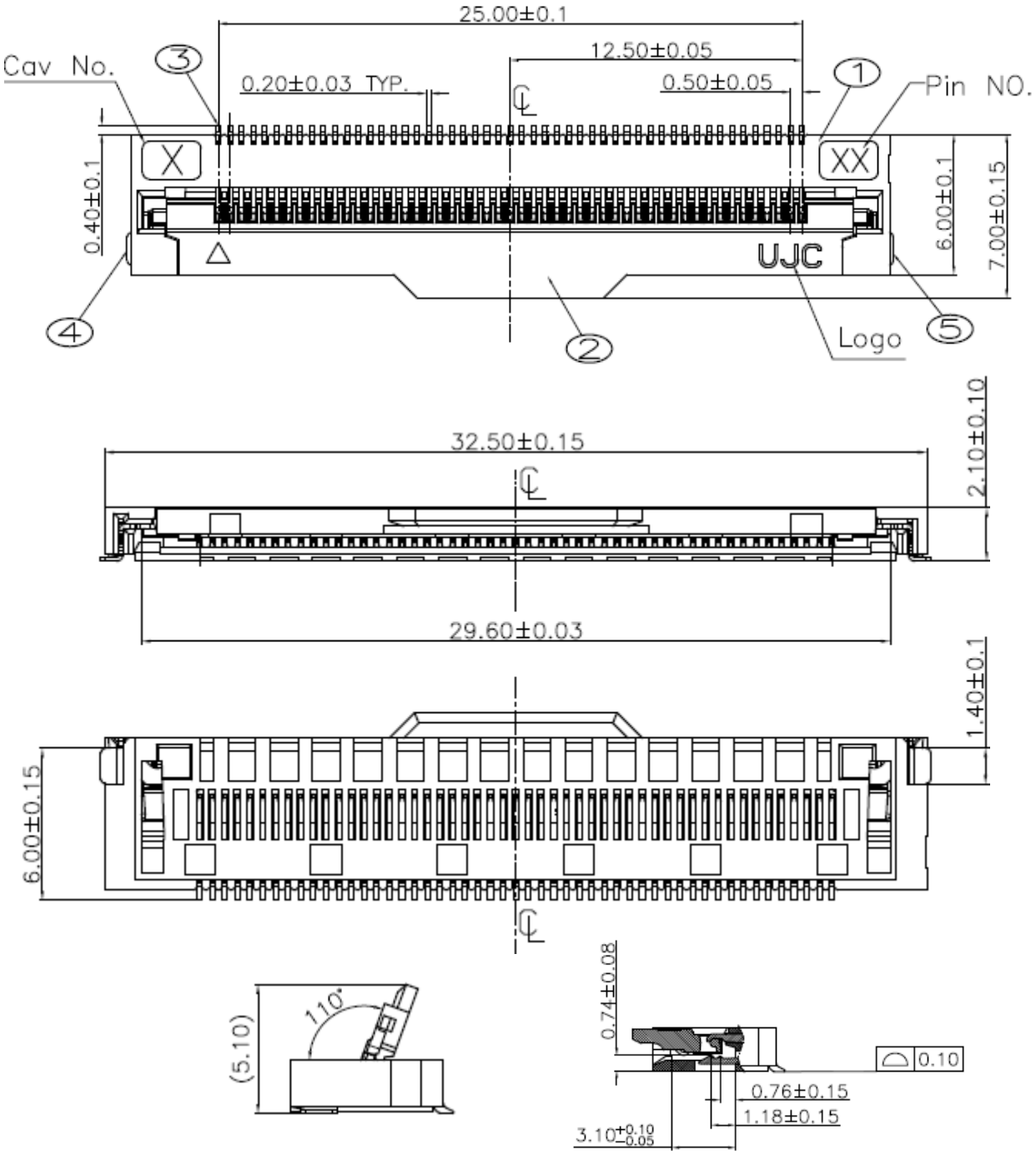
4. Circuit Block Diagram Pin of SDA/SCL.



4.0 INTERFACE CONNECTION

4.4 TCON Board Input CNT &FFC Drawing

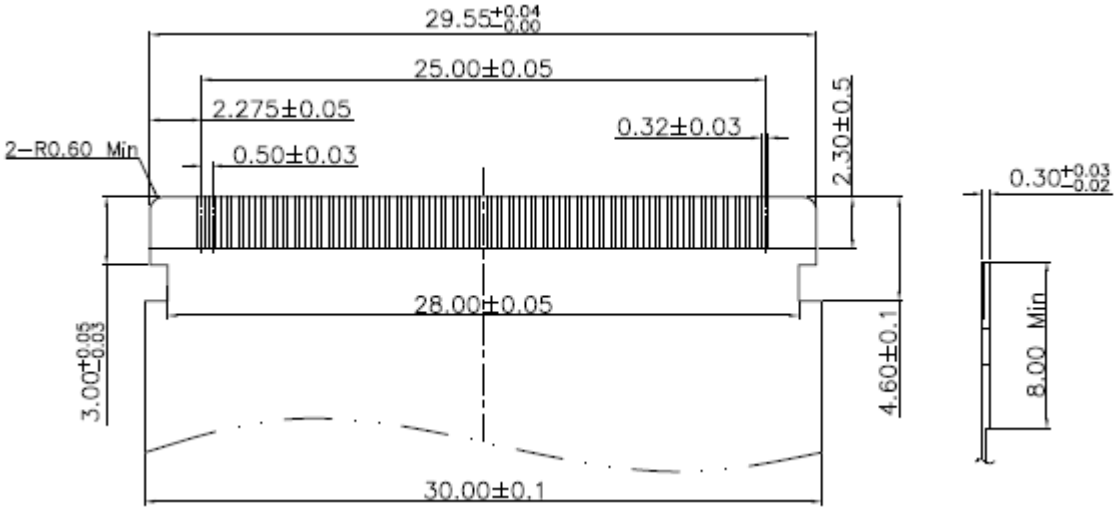
-51pin Connector Drawing-PM.FPC.LVS0505101

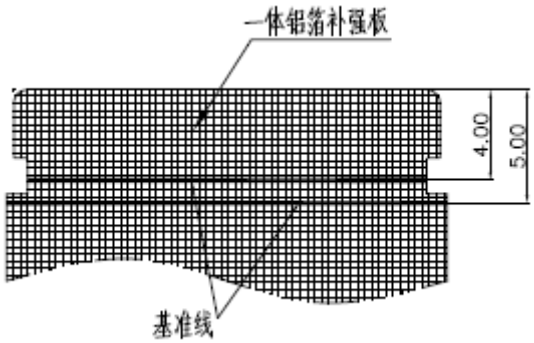


4.0 INTERFACE CONNECTION

4.4 TCON Board Input CNT &FFC Drawing

-FFC Drawing

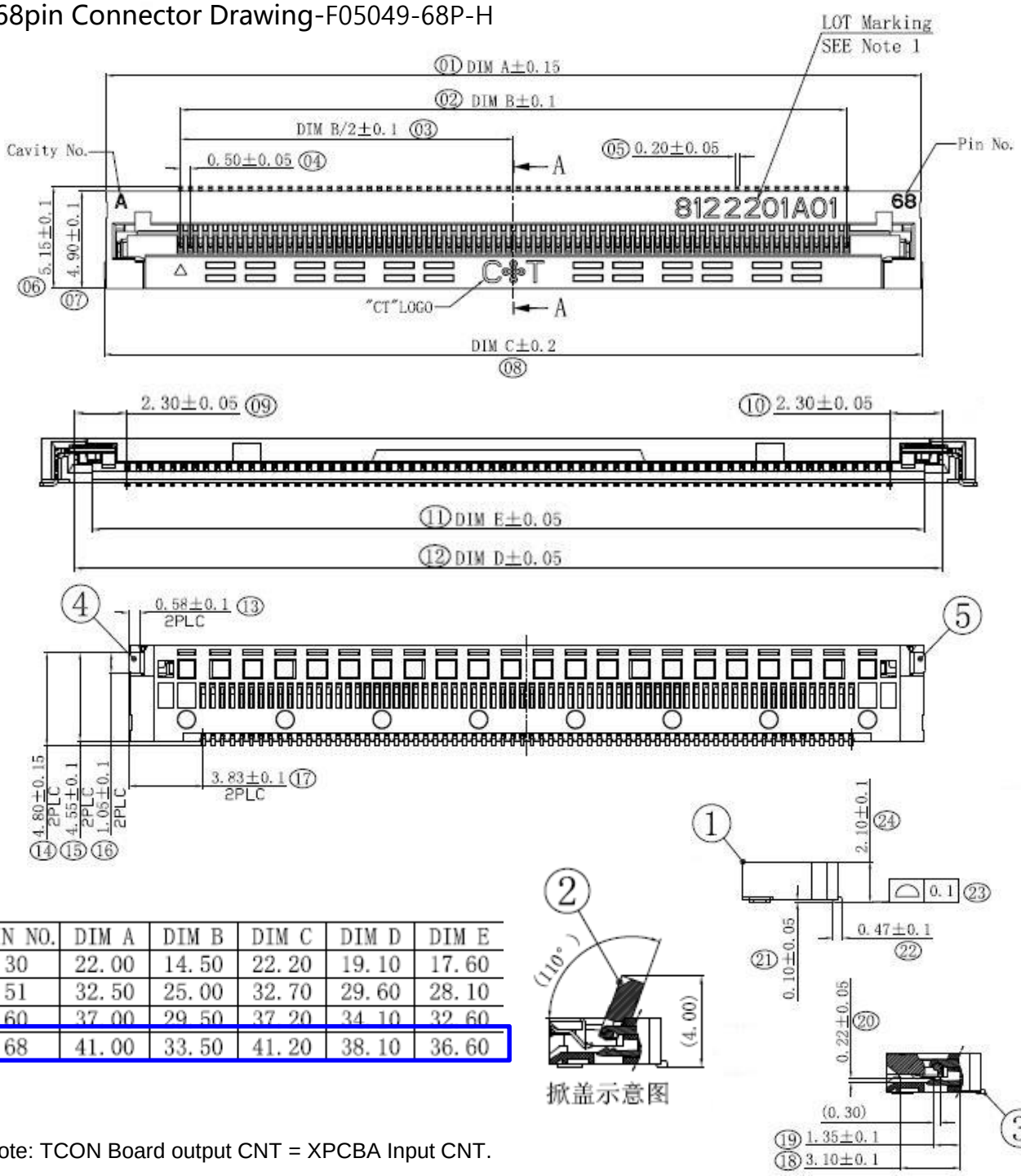




4.0 INTERFACE CONNECTION

4.5 TCON Board Output CNT &FFC Drawing

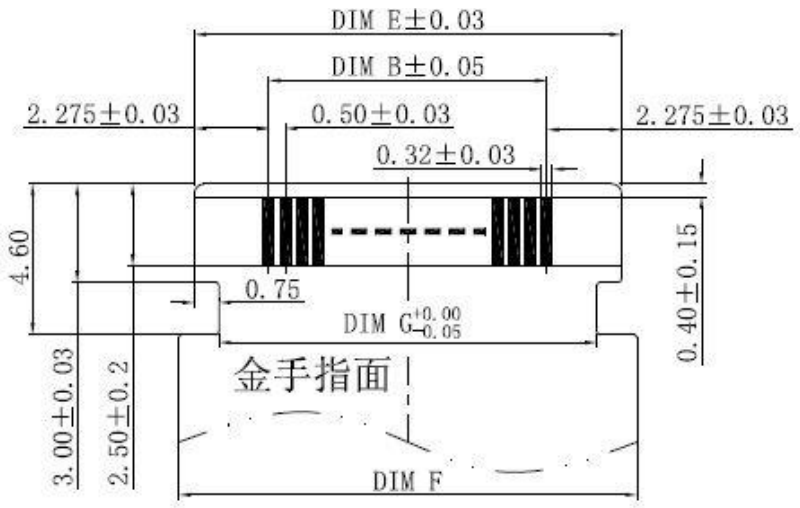
-68pin Connector Drawing-F05049-68P-H



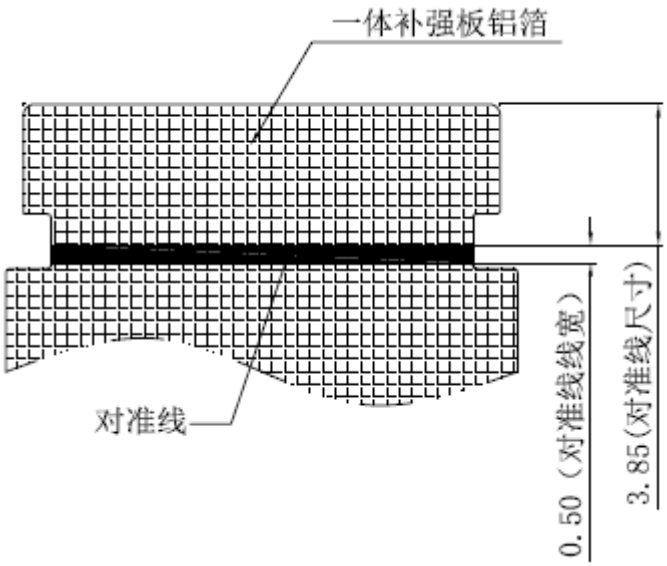
PIN NO.	DIM A	DIM B	DIM C	DIM D	DIM E
30	22.00	14.50	22.20	19.10	17.60
51	32.50	25.00	32.70	29.60	28.10
60	37.00	29.50	37.20	34.10	32.60
68	41.00	33.50	41.20	38.10	36.60

Note: TCON Board output CNT = XPCBA Input CNT.

-FFC Drawing







PIN NO.	DIM B	DIM E	DIM F	DIM G
30	14.50	19.05	20.00	17.55
51	25.00	29.55	30.50	28.05
60	29.50	34.05	35.00	32.55
68	33.50	38.05	39.00	36.55

Notes: This FFC drawing is supplied by the connector vendor.

5.0 SIGNAL TIMING WAVEFORMS OF INTERFACE SIGNAL

5.1 Input data specification

<Table 8. Vx1 Byte length and Color mapping>

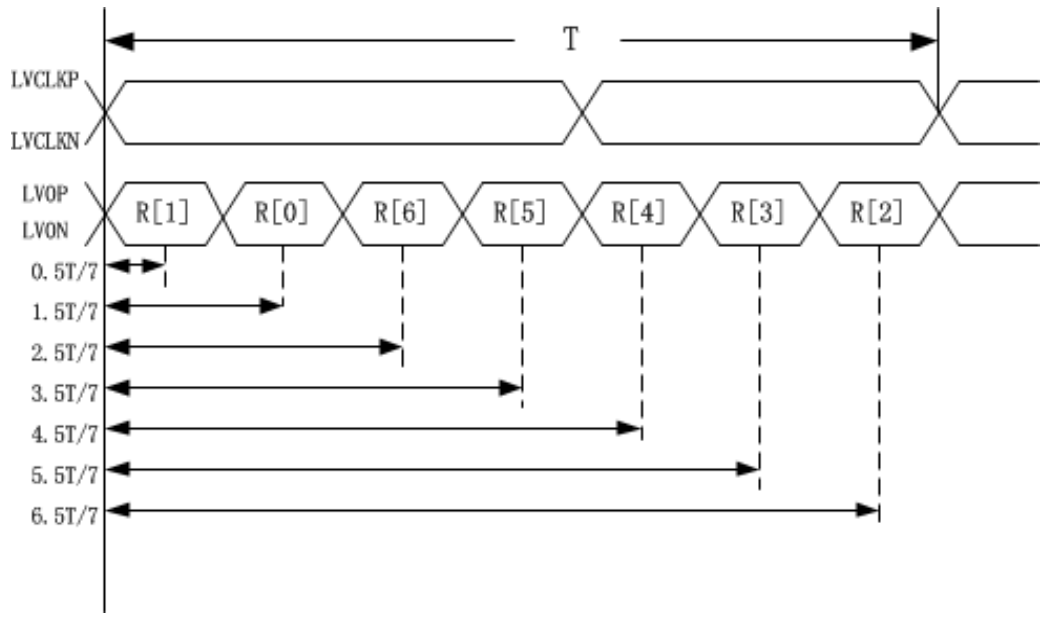
Channel No.	Data No.	8-bit LVDS Type	
		NS	JEIDA
0	Bit-0	R0	R2
	Bit-1	R1	R3
	Bit-2	R2	R4
	Bit-3	R3	R5
	Bit-4	R4	R6
	Bit-5	R5	R7
	Bit-6	G0	G2
1	Bit-0	G1	G3
	Bit-1	G2	G4
	Bit-2	G3	G5
	Bit-3	G4	G6
	Bit-4	G5	G7
	Bit-5	B0	B2
	Bit-6	B1	B3
2	Bit-0	B2	B4
	Bit-1	B3	B5
	Bit-2	B4	B6
	Bit-3	B5	B7
	Bit-4	HS	HS
	Bit-5	VS	VS
	Bit-6	DE	DE
3	Bit-0	R6	R0
	Bit-1	R7	R1
	Bit-2	G6	G0
	Bit-3	G7	G1
	Bit-4	B6	B0
	Bit-5	B7	B1
	Bit-6	-	-

5.2 LVDS Rx Interface Timing Parameter

The Specification of the LVDS Rx interface timing parameter is shown in Table10

< Table 9. LVDS Rx Interface Timing Specification >

Item	Symbol	Min	Typ	Max	Unit	Note
CLKIN Period	T	11.8	13.5	17.9	nsec	
Input Data0	tRCIP1	0.5T/7-0.4	0.5T/7	0.5T/7+0.4	nsec	
Input Data1	tRCIP0	1.5T/7-0.4	1.5T/7	1.5T/7+0.4	nsec	
Input Data2	tRCIP6	2.5T/7-0.4	2.5T/7	2.5T/7+0.4	nsec	
Input Data3	tRCIP5	3.5T/7-0.4	3.5T/7	3.5T/7+0.4	nsec	
Input Data4	tRCIP4	4.5T/7-0.4	4.5T/7	4.5T/7+0.4	nsec	
Input Data5	tRCIP3	5.5T/7-0.4	5.5T/7	5.5T/7+0.4	nsec	
Input Data6	tRCIP2	6.5T/7-0.4	6.5T/7	6.5T/7+0.4	nsec	



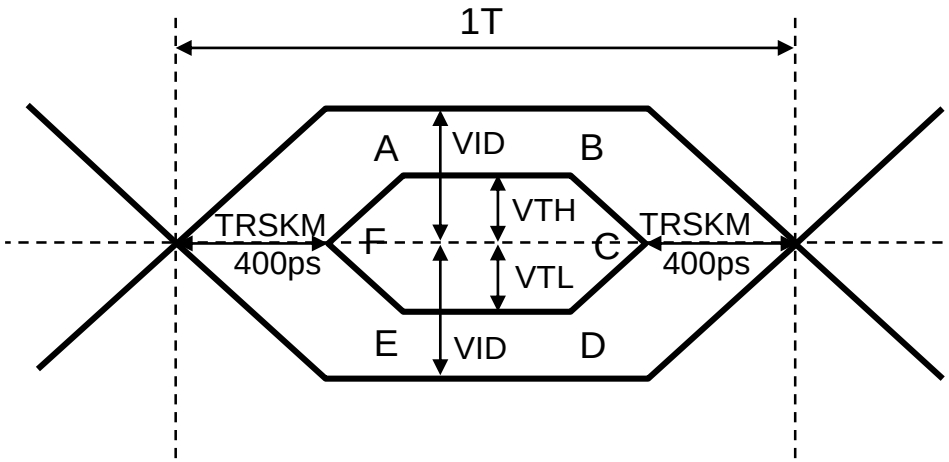
Notes: Input frequency range from 25MHz to 110MHz

5.3 LVDS Rx Interface Eye Diagram & DC SPEC

< Table 10. LVDS DC Specification>

Symbol	Min	Typ	Max	Unit	Remark
A	100	-	-	mV	
B	100	-	-	mV	
C	0	-	-	mV	
D	-100	-	-	mV	
E	-100	-	-	mV	
F	0	-	-	mV	
VTH	+100	-	-	mV	
VTL	-	-	-100	mV	
VID	±100	-	±600	mV	

Notes:
1. TRSKM: 600ps@65MHz, 530ps@74.25MHz, 495ps@79.8MHz，400ps@85MHz.
2. VID /VTH/VTL measure point is below timing. Vid measurement can be judge at the center of Eye.



6.0 SIGNAL TIMING SPECIFICATION

6.1 Timing Parameters(DE only mode)

< Table 11. Timing Table >

Item		Symbols		Min	Typ	Max	Unit
Clock	Frequency	1/Tc		60	74.25	78	MHz
	High Time	Tch		-	4/7Tc	-	
	Low Time	Tcl		-	4/7Tc	-	
Frame Period		Tv		57	60	63	Hz
Horizontal Active Display Term		Valid	t_{HV}	-	960	-	t_{CLK}
		Total	t_{HP}	1060	1100	1200	t_{CLK}
Vertical Active Display Term		Valid	t_{VV}	-	1080	-	t_{HP}
		Total	t_{VP}	1100	1125	1149	t_{HP}

Item		Symbols		Min	Typ	Max	Unit
Clock	Frequency	1/Tc		60	74.25	78	MHz
	High Time	Tch		-	4/7Tc	-	
	Low Time	Tcl		-	4/7Tc	-	
Frame Period		Tv		48.5	50	51	Hz
Horizontal Active Display Term		Valid	t_{HV}	-	960	-	t_{CLK}
		Total	t_{HP}	1060	1100	1200	t_{CLK}
Vertical Active Display Term		Valid	t_{VV}	-	1080	-	t_{HP}
		Total	t_{VP}	1100	1350	1380	t_{HP}

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

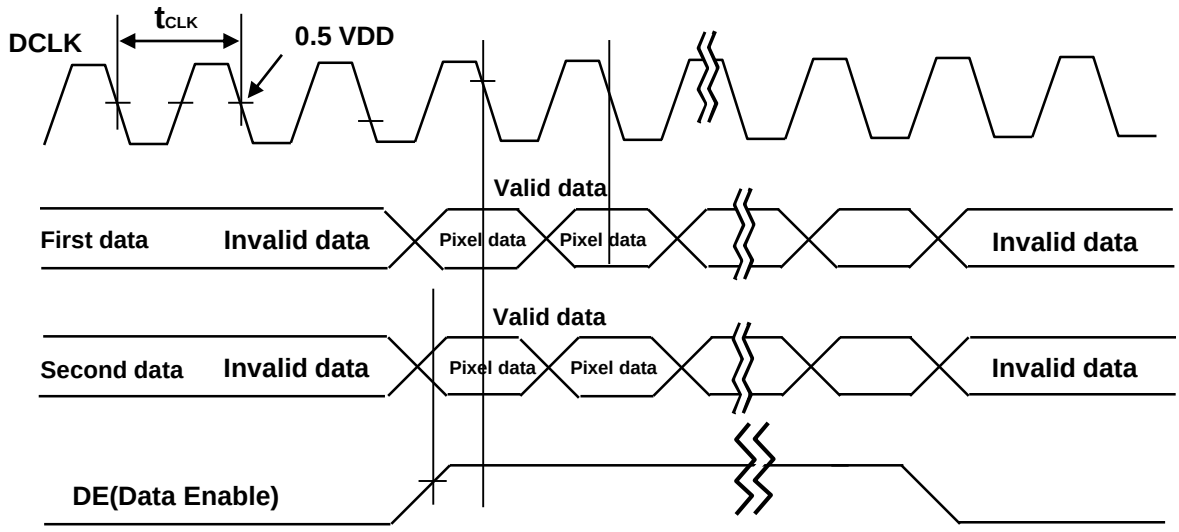
6.0 SIGNAL TIMING SPECIFICATION

6.1 Timing Parameters (DE only mode)

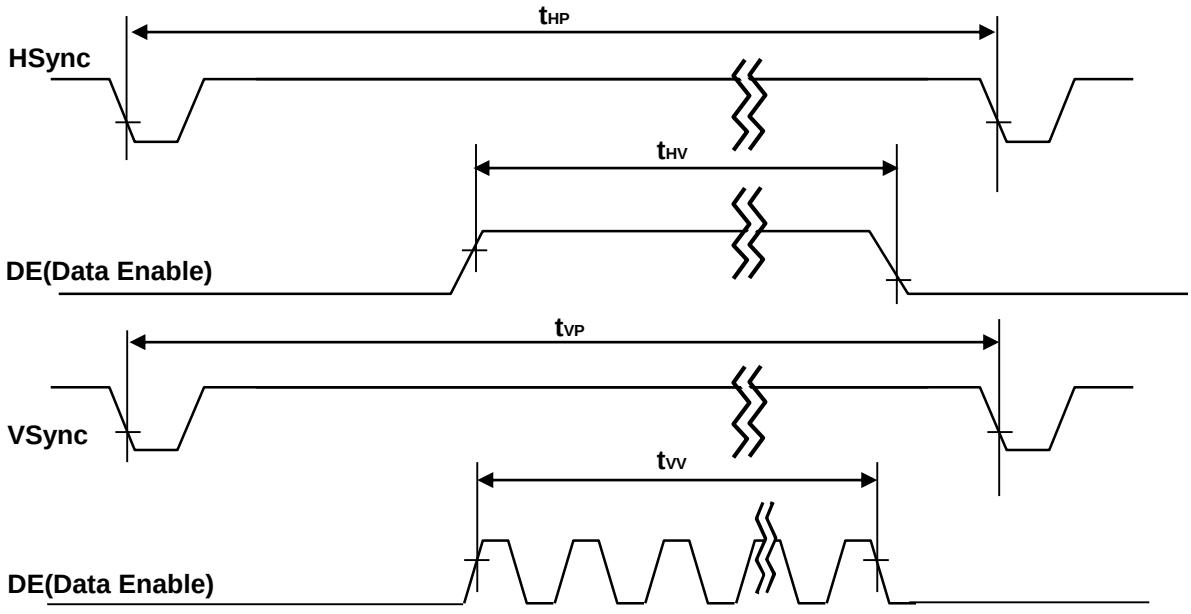
< Table 12. LVDS Input SSCG>

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	60	74.25	78	MHz
T_{LVSK}	LVDS channel to channel skew	F=100MHz V_{IC}=1.2V V_{ID}=±400mV	-380	-	+380	ps
F_{LVMOD}	Modulating frequency of input clock during SSC		-	-	85	KHz
F_{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T_{CY-CY}	Cycle to Cycle jitter		-	-	100	ps

6.2 Signal Timing Waveform



Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.



6.0 SIGNAL TIMING SPECIFICATION

6.3 Input Signals, Basic Display Colors and Gray Scale of Colors

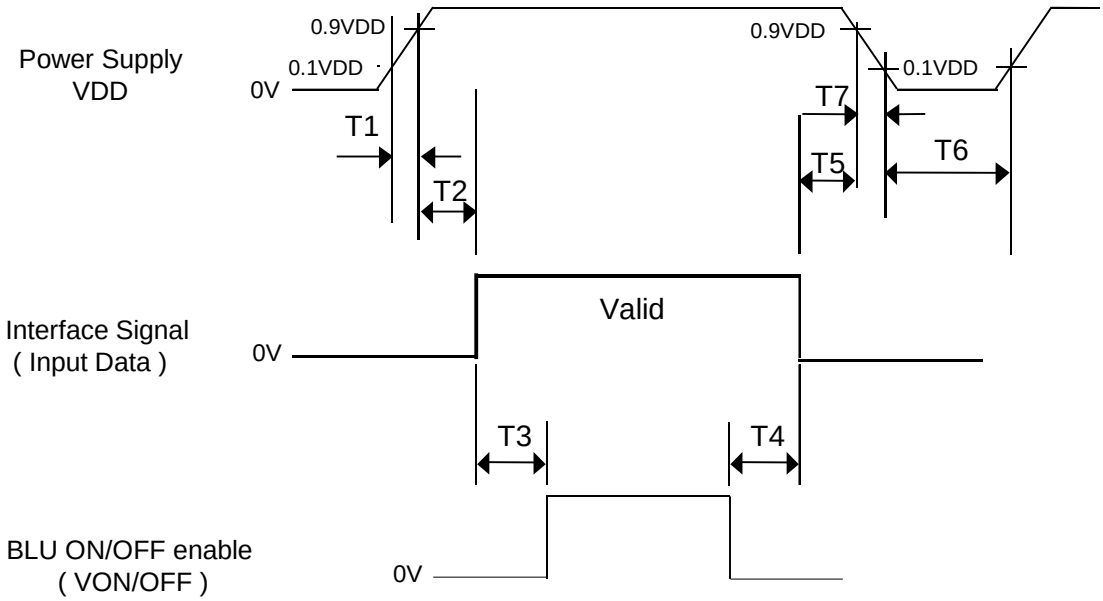
< Table 13. Input Signal and Display Color Table >

Color & Gray Scale		Input Data Signal																							
		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△	↑								↑								↑							
	▽	↓								↓								↓							
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

6.0 SIGNAL TIMING SPECIFICATION

6.4 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



< Table 14. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	10	-	100	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0	-	-	ms
T6	1	-	-	s

Notes: 1. Back Light must be turn on after power for logic and interface signal are valid.
2. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.
3. When VDD<0.9VDD(Typ.),Power off.
4. T7 decreases smoothly, if there were rebounding voltage, it must smaller than 5 volts.

7.0 OPTICAL SPECIFICATION

The test of optical specifications shall be measured in a dark room (ambient luminance≤1 lux and temperature=25±2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

< Table 15. Optical Table >

[VDD = 12.0V, Frame rate = 120Hz, Ta =25±2 ℃]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10	-	89	-	Deg.	-
		Θ_9		-	89	-	Deg.	
	Vertical	Θ_{12}		-	89	-	Deg.	
		Θ_6		-	89	-	Deg.	
Contrast ratio		CR	Θ = 0° (Center) Normal Viewing Angle	800:1	1200:1	-		-
Reproduction of color	White	W_x		TYP. - 0.03	0.278	TYP. + 0.03		Based on BOE Backlight
		W_y			0.285			
	Red	R_x			0.640			
		R_y			0.330			
	Green	G_x			0.305			
		G_y			0.615			
	Blue	B_x			0.154			
		B_y			0.061			
Response Time	G to G	T_g		-	8	10	ms	-
Gamma Scale				2.0	2.2	2.4		
Cell Transmittance				5.67	6.3	6.93	%	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0°$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 15 shall be calculated from the spectral data measured with all pixels first in red, green, blue. Measurements shall be made at the center of the panel. The BLU is used by BOE.
4. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =60Hz to optimize.
   Each time in below table is defined as Figure 2 and shall be measured by switching the input signal for "any level of gray(bright)"and "any level of gray(dark)"

Measured Response Time		Target																
		0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
	255																	

5. Definition of Transmittance (T%) :
   Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100\ \%$$

8.0 MECHANICAL CHARACTERISTICS

8.1 Dimensional Requirements

Figure 3(located in Appendix) shows mechanical outlines for the model HV430QUB-F90. Other parameters are shown in Table 16.

< Table 16. Dimensional Parameters >

Parameter	Specification	Unit
Active area	940.896 (H) × 529.254(V)	mm
Pixel pitch	163.35 (H) ×490.05(V)	μm
Number of pixels	1920(H) ×1080(V) (1 pixel = R + G + B dots)	pixels

9.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

< Table 17. Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs
4	High temperature operation test	Ta = 50 ℃, 240hrs
5	Low temperature operation test	Ta = 0 ℃, 240hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle

This test condition is based on BOE module.

10.0 HANDLING & CAUTIONS

(1) Cautions when taking out the Panel

- Pick the pouch only, when taking out panel from a shipping package.

(2) Cautions for handling the panel

- As the electrostatic discharges may break the LCD panel, handle the LCD panel with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD panel should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD panel is operating.
- Put the panel display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation

- When the panel is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the panel would be damaged.

(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD panel in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

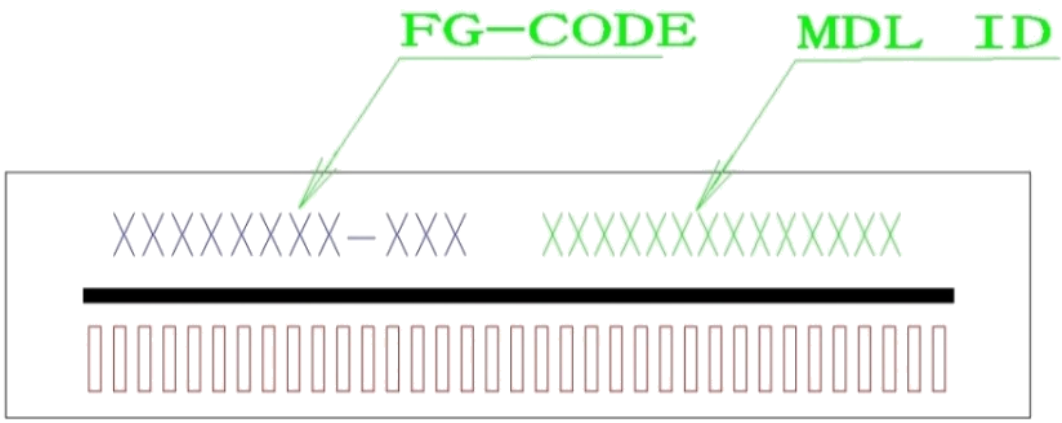
(5) Cautions for the panel characteristics

- Do not apply fixed pattern data signal to the LCD panel at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions

- Do not disassemble and/or re-assemble LCD panel.
- Do not re-adjust variable resistor or switch etc.
- When returning the panel for repair or etc., Please pack the panel not to be broken. We recommend to use the original shipping packages.

11.0 PRODUCT SERIAL NUMBER



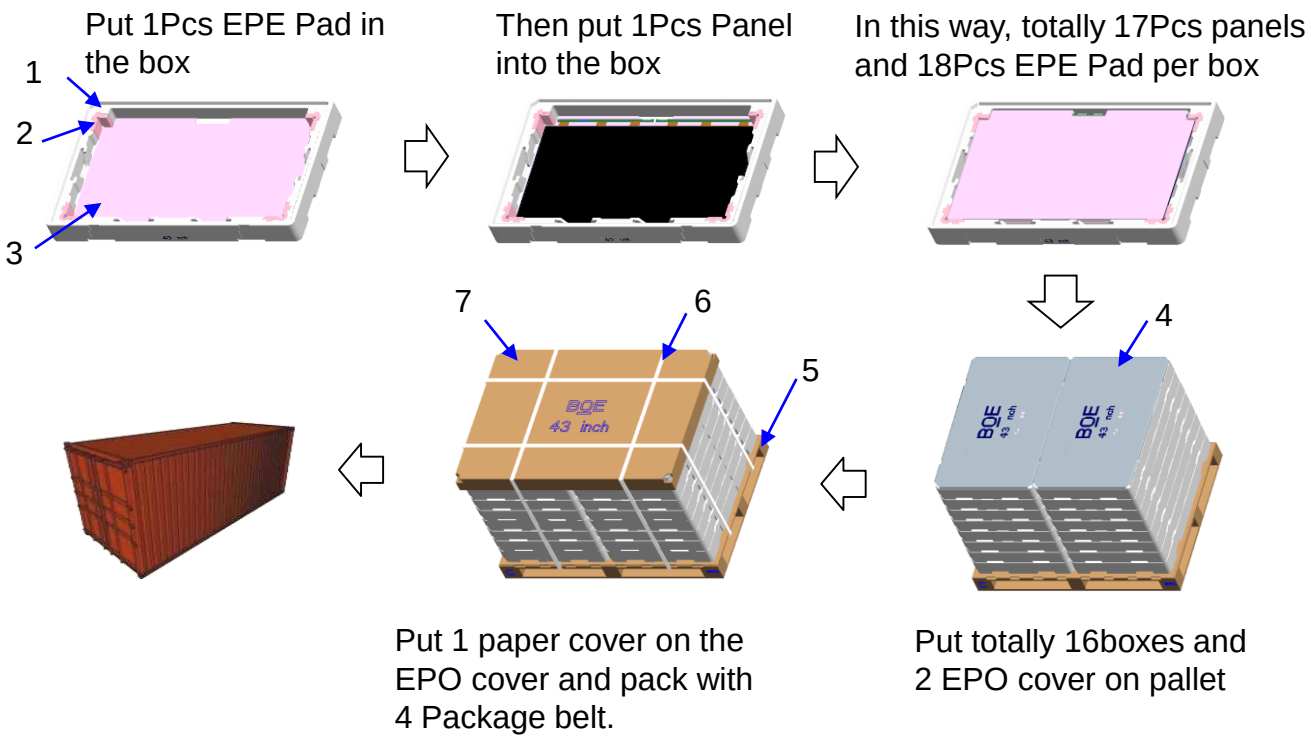
MDL ID Naming Rule:

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	S	L	S	9	1	6	3	5	9	4	2	0	A	A	0	0	0
Description	Model Code /GBN		Grade	Line	Year		Month	Model Extension Code (Last 4 Digits Of FG-CODE)				Serial No 00001-ZZZZZZ					

12.0 PACKING

BOE provides the standard shipping container for customers, unless customer specifies their packing information. The standard packing method and Barcode information are shown in below.

12.1 Packing Order



Cautions: When transferring in warehouse or factory, the arm length of electric forklift or hand pallet truck must be longer than the pallet.

No.	Description	Material
1	Bottom	EPO
2	Cushion	EPP
3	Pad	EPE
4	Cover	EPO
5	Pallet	Wood+ Paper+ PE
6	Band	PP
7	Cover	Paper

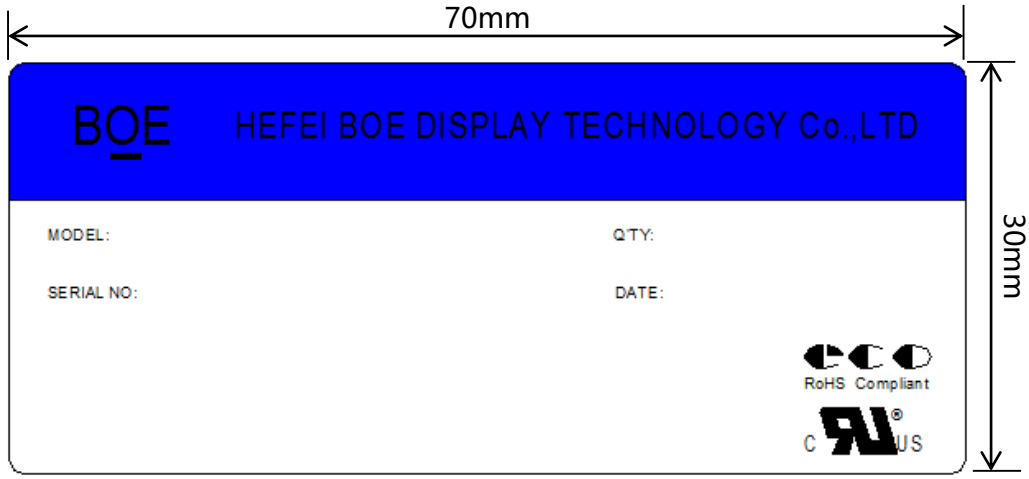
12.2 Packing Note

- Box Dimension : 1100(±3)mmL×705(±2)mmW×127(±1.5)mmH
- Package Quantity in one Box : 17pcs

12.3 Box Label

- Label Size : 70 mm (L) × 30 mm (W)
- Contents

  Model : HV430FHB-F90 （FG Code of Product）
  Q`ty : 17 Open Cell in one box.
  Serial No. : Box Serial No.
  Date : Packing Date



Box ID Naming Rule:

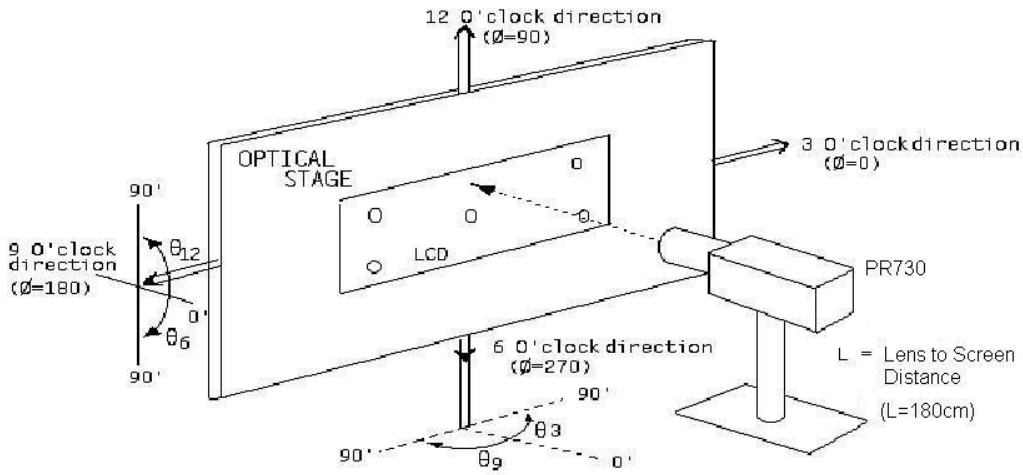
Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	S	L	S	9	1	6	3	5	9	4	2	0	0
Description	Products GBN		Grade	Line	Year		Mon th	Revision Code	Serial No 00001-ZZZZZZ				

12.4 Packing Material ESD Specification

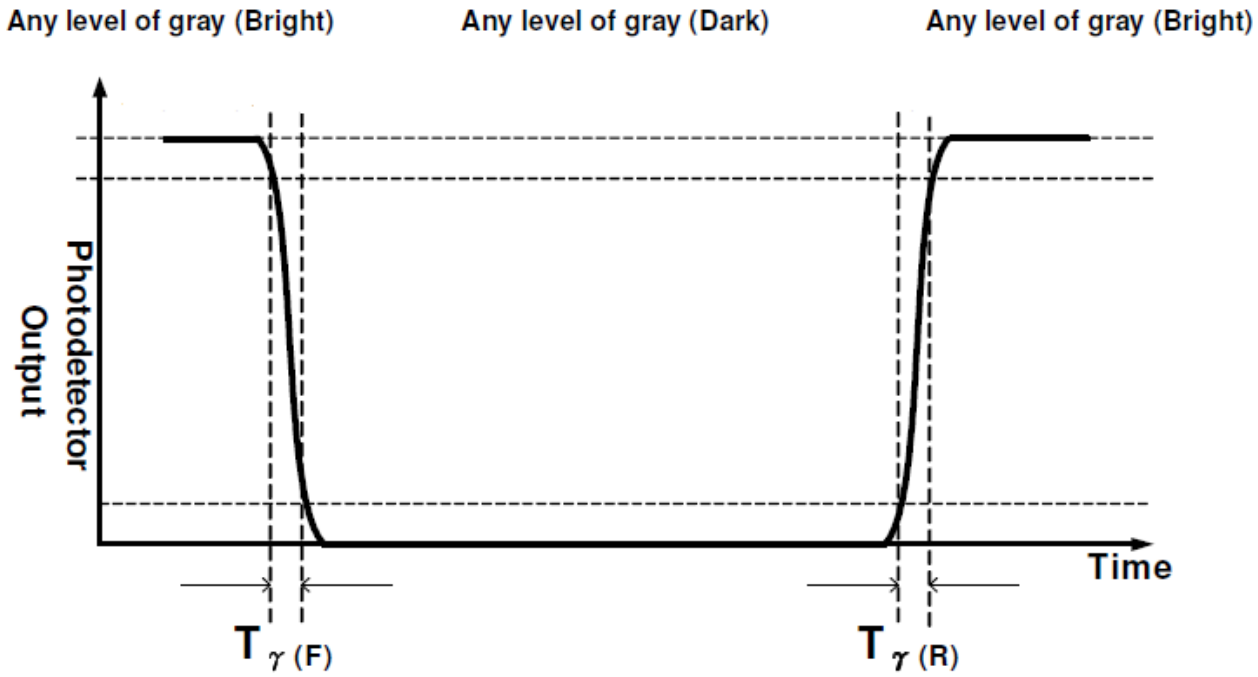
Item	SPEC
Surface Resistance [10^n Ω]	Control by 10^{6}~10^{11} - Box, Spacer

13.0 APPENDIX

< Figure 1. Measurement Set Up >

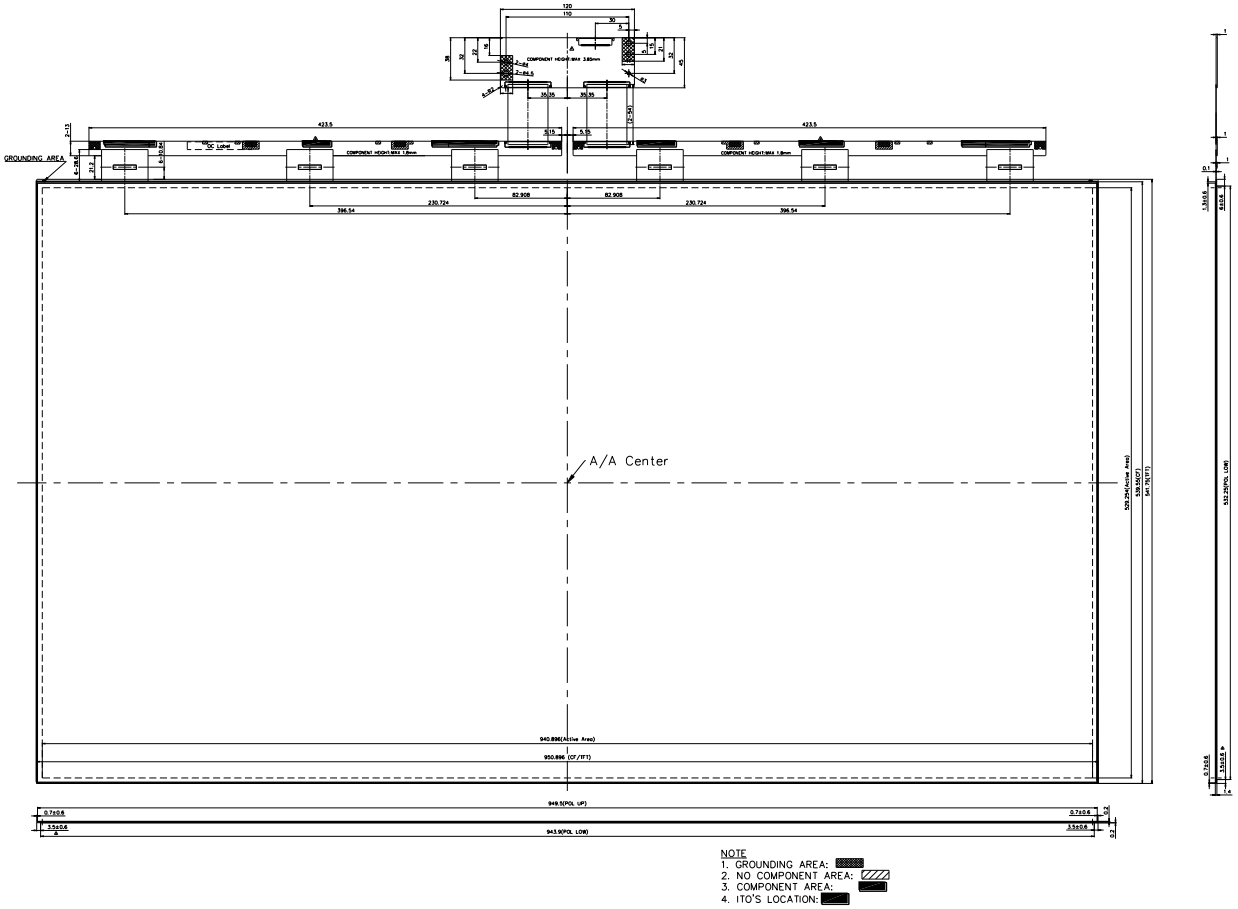


< Figure 2. Response Time Testing >



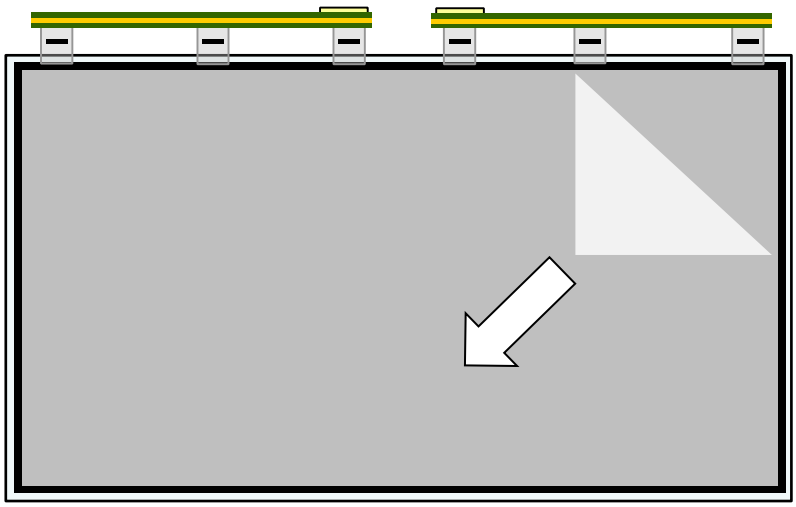
13.0 APPENDIX

< Figure 3. TFT-LCD Open Cell Outline Dimensions (Front View) >



13.0 APPENDIX

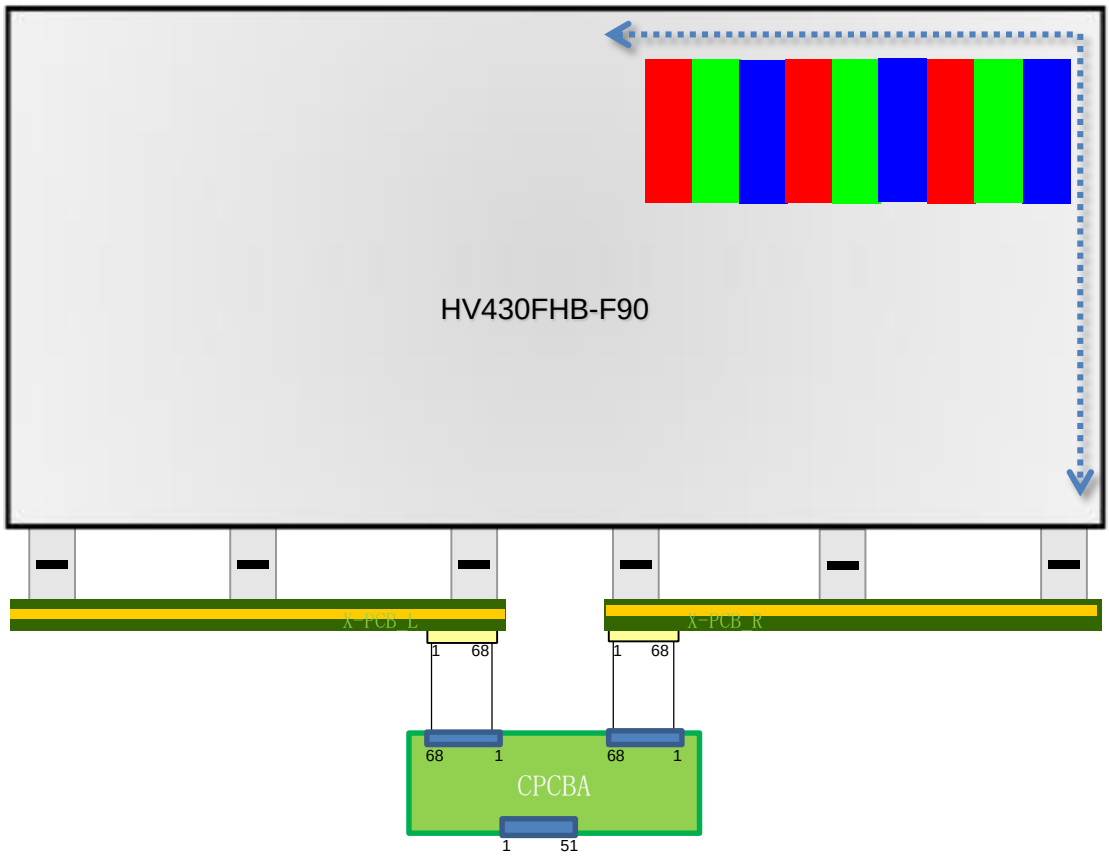
< Figure 4. TFT POL Protect Film Peeling Method >



1. Be sure to peel off slowly(recommended more than 7sec) and constant speed.
2. Peeling direction shows in Figure 4.
3. Be sure to ground person with adequate methods such as the anti-static wrist band.
4. Be sure to ground each S-PCB while peeling off the protection film.
5. Ionized air should be blown over during peeling action.
6. The protection film must not touch drivers and S-PCBs.
7. If adhesive may remain on the polarizer after the protection film peeling off, please rem ove with isopropyl-alcohol.

13.0 APPENDIX

(a)This Product is Reverse type display Mode



1. Panel scan direction is from top to bottom.
2. Driver data latch direction is from right to left.